IN THE CLAIMS

The following listing of claims replaces all previous listings and versions of claim in this application.

1. (withdrawn) A semiconductor structure comprising: a substrate having a surface and being made of a material that provides a typical surface properties to the surface; a bonding layer located on the surface of the substrate; and a further layer molecularly bonded to the bonding layer.

2. (withdrawn) The structure of claim 1 wherein the atypical surface properties comprise at least one of a roughness of more than 0.5 nm rms, or a roughness of at least 0.4 nm rms that is difficult to polish, or a chemical composition that is incompatible with molecular bonding.

3. (withdrawn) The structure of claim 1 wherein the substrate has a thermal conductivity of more than 1 W/cm/K.

4. (withdrawn) The structure of claim 1 wherein the substrate comprises diamond or aluminum nitride material.

5. (withdrawn) The structure of claim 1 wherein the substrate material comprises an intermediate layer that provides the surface having the atypical surface properties and the bonding layer that has a thermal conductivity that is higher than that of the substrate or that is between that of the bonding layer and that of the substrate.

6. (withdrawn) The structure of claim 5 wherein the intermediate layer is silicon nitride.

7. (withdrawn) The structure of claim 1 wherein the thickness of the bonding layer is in the range of about 5 nm to about 20 nm.

8. (withdrawn) The structure of claim 1 wherein the bonding layer comprises at least one of silicon dioxide (SiO_2), silicon nitride (Si_3N_4), hafnium oxide, zirconium oxide, alumina, or yttrium oxide.

9. (withdrawn) The structure of claim 1 wherein the further layer is a semiconductor material comprising at least one of silicon, germanium, gallium arsenide, silicon-germanium, a semiconductor Group III-Group V material, or a semiconductor Group II-Group VI material.

10. (withdrawn) The structure of claim 9 wherein the structure is a Semiconductor-On-Insulator (SOI) structure.

11. (withdrawn) The structure of claim 9 wherein at least one portion of a surface of the bonding layer facing the further layer is positioned at a distance of 10 nm or less from the surface of a peak of the substrate to optimize heat transfer from the further layer to the substrate.

12. (withdrawn) The structure of claim 9 which further comprises at least one power component or radio frequency (RF) component in the further layer of semiconductor material.

13. (withdrawn) The structure of claim 9 which further comprises at least one insulated gate bipolar transistor (IGBT) component or metal oxide on silicon field effect transistor (MOSFET) component in the further layer of semiconductor material.

14. (withdrawn) The structure of claim 1 wherein the further layer is a second substrate of a material having a typical surface properties.

15. (withdrawn) The structure of claim 14 wherein the atypical surface properties of the second substrate comprise at least one of a roughness of more than 0.5 nm rms, or a roughness of at least 0.4 nm rms that is difficult to polish, or a chemical composition that is incompatible with molecular bonding.

16. (original) A method for fabricating a semiconductor structure comprising: providing a substrate having a surface and being made of a material that provides a typical surface properties to the surface; providing a bonding layer on the surface of the substrate; smoothing the bonding layer to provide a surface that is capable of molecular bonding; and molecularly bonding a further layer to the bonding layer to form the structure.

17. (original) The method of claim 16 wherein the atypical surface properties comprise at least one of a roughness of more than 0.5 nm rms, or a roughness of at least 0.4 nm rms that is difficult to polish, or a chemical composition that is incompatible with molecular bonding.

18. (original) The method of claim 16 which further comprises forming an intermediate layer on the substrate to provide the surface layer having the atypical properties before providing the bonding layer, the intermediate layer having a thermal conductivity coefficient that is higher than that of the substrate or that is between that of the bonding layer and that of the substrate.

19. (original) The method of claim 18 wherein the intermediate layer is composed of silicon nitride.

20. (original) The method of claim 16 wherein the thermal conductivity of the substrate is more than 1 W/cm/K.

21. (original) The method of claim 16 wherein the substrate material comprises at least one of diamond or aluminum nitride.

22. (original) The method of claim 16 wherein the bonding layer material comprises at least one of silicon dioxide, silicon nitride, hafnium oxide, zirconium oxide, alumina or yttrium oxide.

23. (original) The method of claim 16 wherein the further layer is made of a semiconductor material.

24. (original) The method of claim 23 which further comprises producing at least one of a power component and a radio frequency (RF) component in the further layer.

25. (original) The method of claim 16 wherein the further layer is a second substrate of a material having a typical surface properties.

26. (original) The method of claim 25 wherein the atypical surface properties of the second substrate comprise at least one of a roughness of more than 0.5 nm rms, or a roughness of at least 0.4 nm rms that is difficult to polish, or a chemical composition that is incompatible with molecular bonding.

27. (original) The method of claim 25 which further comprises providing a second bonding layer on the second substrate before molecularly bonding.

28. (original) The method of claim 25 wherein the second substrate comprises at least one of diamond or aluminum nitride.